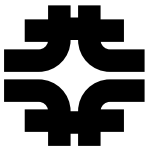

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Protocols and Standard Crate Configuration For a Typical CDF Run 2 Readout Crate

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Abstract

This paper describes a standard for the readout and the trigger interface of a VMEbus based crate to be used by the front-end and trigger electronics of the CDF Run 2 experiment. Hereafter, this crate will be referred to as the CDF Readout Crate. The goal is to standardize the implementation of functions that are common among all systems (i.e. power distribution, timing signals, DAQ functions) while allowing some flexibility with other functions (e.g. cooling, rear transition modules, J3 backplanes, etc.). This allows designers of cards that satisfy this standard to have access to a common well defined crate system with interfaces to the trigger and DAQ system, allowing them to concentrate their efforts on the functions they need. This paper lists the mechanical specifications, readout scheme, backplane and signal distribution specifications of the CDF Readout Crate. The paper will also go into some detail on the **TR**igger **A**nd **C**lock + **E**vent **R**eadout (TRACER) module, a common CDF crate module which provides the crate interface to the system clock and the trigger system.

I. INTRODUCTION

The data acquisition architecture for the CDF Run 2 experiment[1] required a significant upgrade for the readout crate capability over the Rabbit crate used in Run 1. The Rabbit system[2] was designed for low noise and had no readout activity occurring during data acquisition. This type of readout was acceptable with crossing rates of 3.5 us, but would not work with the Run 2 crossing time of 132 ns and a readout which was designed with a deadtimeless approach.

The crate selected for Run 2 would have to allow for simultaneous data conversion and readout. The readout bandwidth would have to approach 10 MB/s for some front end crates.

II. MECHANICAL SPECIFICATIONS

The selection of a crate for the Run 2 experiment began with a survey of what was commercially available and easily adaptable for our purposes.

A. Selection of VMEbus

VMEbus[3] seemed to be commercially popular, met the bandwidth requirement, and had enough flexibility through the provision of many user-defineable pins that we felt we could adapt VMEbus for our purposes. One positive aspect of selecting a commercially available bus, was that we could immediately go out and buy a powerful and inexpensive VMEbus Crate Controller (VRC).

The standard 6U x 160 mm card format used by VMEbus was too small for our purposes, and we decided to use a 9U x 400 mm format. To help handle crate I/O, we also decided upon a 9U x 100 mm transition (rear) card format. Crates could still be commercially purchased for cards this size.

The standard VMEbus backplane contains 64 user-definable signal pins per slot on the J2 backplane. We made the decision to bus these lines across slots 2-21 of the VMEbus backplane. These bussed lines provide all clock and trigger information required to run the experiment. Slot 1 was reserved for the VRC, and was left as a VMEbus standard slot.

The J3 portion of the backplane was left separate from the monolithic J1/J2 backplane and was allowed to be fully customizable. This allows separate detector systems to define the backplane as best fit their needs.

A Custom 6U to 9U Adapter module[4] was quickly designed, which allowed us to safely use commercial 6U modules in our crate. The custom adapter provided fusing and isolated commercial 6U modules from the user-defined pins which we were now using. We, therefore, had a working prototype of the crate with a readout controller in very short order.

At this point, CDF joined and helped spearhead the effort of the VIPA[5] committee in designing a crate for high energy physics.

B. Selection of CDF VIPA standard

The VIPA committee began to define a crate by looking at the general needs of the high energy physics community and the specific needs of CDF. A 10U crate was conceived and defined which would house 9U x 400 mm cards, allow for 9U x 100 mm transition modules, provide module/slot keying and provide non-standard VMEbus power for physics applications.

The crate made use of new 5-row VMEbus connectors which were developed for the VME64Extensions[6] standard. These connectors brought in many additional ground pins. This was vital to holding down digital noise and making precision analog work possible in the crate.

A CDF version of the VIPA crate bussed the 64 user-defined signals of the J2 backplane from slot 2-21. The VIPA

[1]Work supported by the U.S. Department of Energy under contract No. DE-AC02-76CH03000.

crate makes use of a P0 connector to bring in additional +5 Volt power, in addition to 4 user-defined "analog" voltages.

C. Power

The 10U VIPA crate uses the extra 1U (on top of the 9U card format) to bring in the standard +5 Volts, +/-12 Volts, +3.3Volts defined in the VME64Extensions document, as well as 4 additional user-defined voltages and returns which can be used to power analog applications.

The mechanics of bringing in the crate power is done in such a way that all 21 transition slots may be used. Non-standard VMEbus power is supplied to the cards through the VIPA defined P0 connector.

III. READOUT AND TRIGGER INTERFACE

The readout and trigger interface for the typical front end crate is accomplished using two modules in slots 1 and 2, as shown schematically in figure 1. A commercially available CPU (i.e. Motorola's MVME2301[7]) will be used as the VMEbus Readout Controller (VRC) in slot 1. A custom module for trigger interface, crate monitoring and event readout (TRACER[8]) is in slot 2.

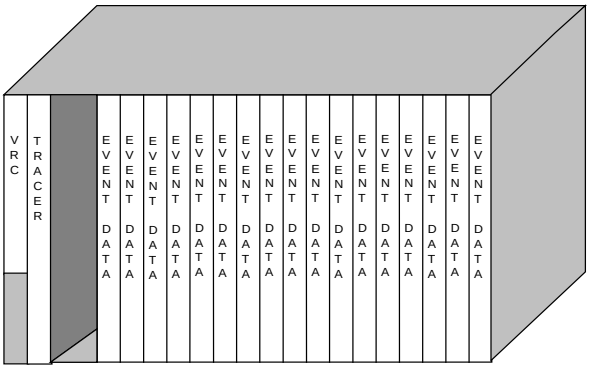

Figure 1. Typical CDF Readout Crate has VRC in slot 1, TRACER in slot 2, and custom electronics in slots 3 – 21.

The VRC will readout event data in the crate using 32 bit block transfers. Communication with the VRC for the downloading of programs and data and diagnostic functions will be accomplished through an ethernet connection. At run initialization time, four DMA tables used in the block transfers are downloaded to the VRC. The four DMA tables correspond to the four L2 Decision buffers. The setup overhead for a block transfer then involves pointing to the appropriate DMA table, based on the L2 Decision buffer to be read out. Figure 2 illustrates the control and data communication paths with the front end crate are accomplished mainly through the TRACER module.

A. The Trigger System

The Trigger System Interface (TSI)[9] sends commands down to the front end crate which indicate what is to be done with event data. Each data taking front end board implements a 42 stage pipeline holding about 5.5us (42 x 132ns) of data. The TSI is responsible for sending a trigger decision every 132ns which corresponds to the data coming off the end of the pipeline. Each front end module contains four L2 Decision buffers to hold data selected for readout. The TSI will also initiate and direct the readout of the data which passes CDF triggers.

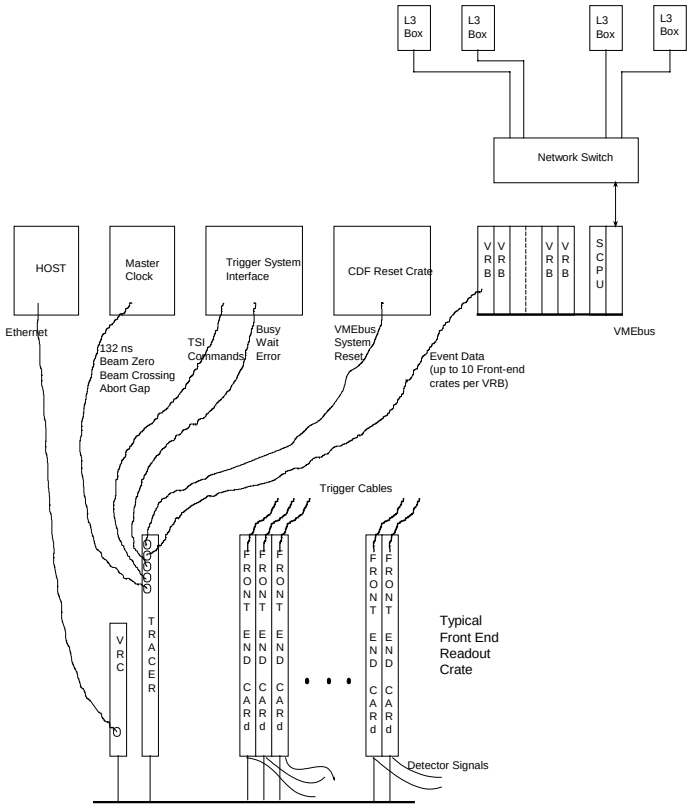

Figure 2. Block Diagram of Readout Architecture

The TSI issues its commands to the front end crate through an optical link with the TRACER. The link uses serializing TAXIchips operating at 136 Mb/s. The TRACER interprets the commands received from this link and passes them to the other front end boards via the bussed lines of the J2 backplane.

The TRACER also uses a parallel copper link (Category 5 cable) to pass crate status information up to the TSI. The TRACER monitors data flow and readout. The TRACER sends back a DONE signal when Readout is complete, a BUSY signal which indicates that the TSI must throttle data transmission, and an ERROR which indicates that some catastrophic error has occurred within the crate.

B. The Master Clock

The Master Clock[10] provides four signals to the typical Readout Crate. A precision 132 ns clock in addition to a Beam Crossing, Beam Zero and Abort Gap marker are sent to the crate through a front panel connection to the TRACER.

The only precision signal distributed on the backplane is CDF_CLOCK, the 132 ns clock used in CDF Run 2. All other trigger and clock signals are considered gates to the rising edge

of CDF_CLOCK. A 10 ns setup and hold time for all gated signals is guaranteed on the backplane, as shown in Figure 3.

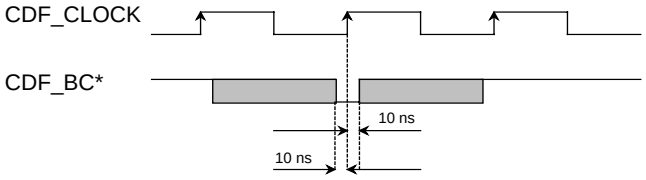

Figure 3. The rising edge of CDF_CLOCK validates all gated clock and trigger signals.

C. The Reset Crate

The CDF Reset Crate[11] also has a connection to all CDF readout crates. The Reset Crate has a copper link to the TRACER front panel which allows the user to remotely issue a VMEbus system reset via the TRACER. This connection allows us to reboot the VRC in event of the board hanging.

D. The Tracer

The **Tr**igger **A**nd **C**lock + **E**vent **R**eadout (TRACER) module has multiple functions. A simple functional block diagram of the TRACER is seen in Figure 4.

One TRACER function is to collect the data, as a "spy" on the VMEbus backplane, during block transfers under control of the VRC. The TRACER transmits collected data serially to VMEbus Readout Buffer (VRB)[12] modules. (Alternatively, the VRC may read in the event data, do zero suppression, and write the formatted data directly into the TRACER's Event FIFO). The TRACER utilizes the serial TAXIchip protocol and fiber optics to transmit data from its Event FIFO to the VRB at up to 15MB/s out of the crate.

As a second function, the TRACER will append an event header to the data stream. This header includes crate, partition and event identification, as well as the buffer number being read out.

The TRACER provides communication to the Trigger Supervisor Interface. It receives all control signals sent by the TSI and fans out the trigger signals required by data taking modules onto the CDF custom J2 backplane.

The TRACER also provides all return signals required by the TSI. These include a DONE, which signals VRB readout is complete, BUSY, which indicates the VRB buffers are in danger of overfowing, and ERROR, which indicates a catastrophic error has occurred in the CDF readout crate.

The TRACER receives the CDF clock signals from the master clock. The TRACER runs the 132 ns clock through a phase lock loop to provide a 50% duty cycle signal. The TRACER then drives the CDF 132 ns clock and its associated gates (a once around marker, a beam crossing indicator, and an abort gap marker) onto the J2 backplane.

Additionally, the TRACER contains the Start Scan register (Start Scan is received from the TSI to initiate event readout) which is polled by the VRC (alternatively an interrupt to the VRC may be generated), and a DONE register (DONE is sent to TSI to indicate VRC readout is complete) which will be written by the VRC. These registers provide the information for the Start Scan - Done handshake between the CDF Readout Crate and TSI systems.

E. The VMEbus Readout Buffer Module

The VRB module acts as a large FIFO device which merges and concentrates up to ten serial data streams sent from individual TRACER modules. The TRACER to VRB link uses the TAXIchip technology to serialize the data and the transmit it over an optical link.

Once the data from up to ten front end crates is concentrated in a single VRB, the data is read out and sent through a network switch into a Level 3 processing farm.

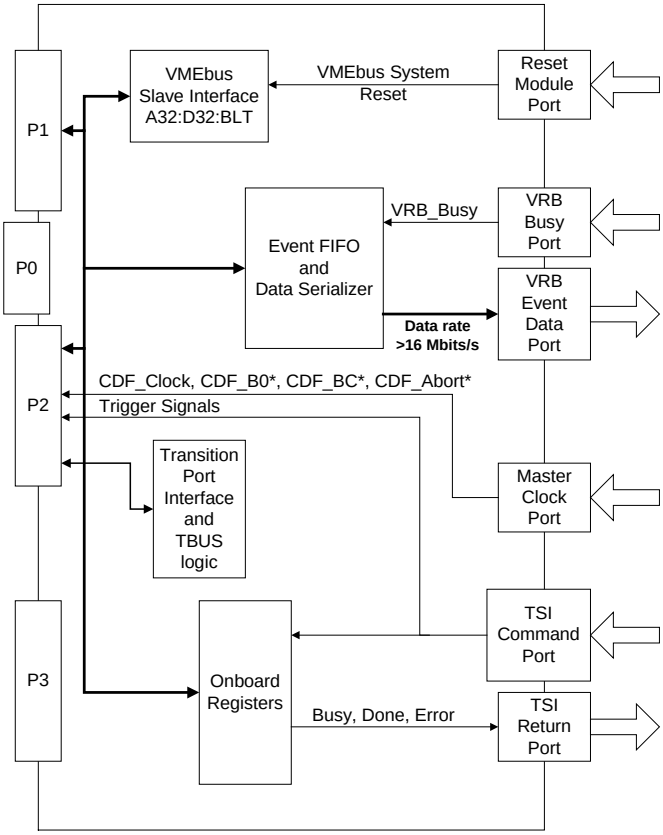

Figure 4. Block diagram of TRACER functionality.

F. Data Readout

The readout of event data proceeds as follows:

- The clock and timing signals from the clock are received by the TRACER and fanned-out on the J2 backplane.
- Modules receive the timing signals and process the data appropriately (e.g. integrate and sample the calorimeter energy).

- The data is placed in a L1 pipeline awaiting a Level 1 accept or reject from the TSI along the J2 backplane via the TRACER.
- A level 1 reject causes the data to be thrown out. An accept comes with a 2 bit address which tells the module which of the four L2/DAQ buffers the data for this L1 accept should be directed too.
- If the event is rejected by level 2, the TSI can send that L2 Decision buffer address for subsequent L1 accepts.
- If the event is accepted by Level 2, the TSI can send a Start Scan message along with the two bits indicating which of the L2 Decision buffers is to be read out. This information is received by the TRACER and stored in a "Start Scan register".
- The VRC polls the Start Scan register (or receives an interrupt driven by TRACER) in the TRACER module. If it is set, it uses the two bits indicating the L2 Decision buffer address to look up the appropriate one of the four DMA block transfer tables in the VRC.
- The VRC initiates its 32 bit block transfers of the event data in the VMEbus modules.
- As the data appears on the VMEbus during the block transfers under control of the VRC, the TRACER module picks the data off the VMEbus (hence the phrase SPY) and transmits it serially to a VRB module. Alternatively, the VRC may take in the Event data, do zero suppression, and then write the formatted Event data directly to the TRACER's Event FIFO, where it is serialized and sent to a VRB.
- On completing the DMA block transfers the VRC writes a Done message to the DONE register in the TRACER module and clears the Start Scan register in the TRACER module.
- The TRACER transmits the DONE message to the TSI.
- When the entire detector is done reading out, another Start Scan message can be sent to the TRACER and the process repeated.

IV. Signal Distrubution

All CDF Run 2 specific signals are distributed are distributed on a special J2 backplane which busses 64 user definable pins. These signals are used to distribute trigger decisions and commands as well as the 132 ns system clock.

The 132 ns clock is distributed as a differential PECL signal. An general ERROR line is treated as open-collector, to allow any module to pull it down and indicate a problem within the crate. All other CDF signals are active low and use TTL levels.

V. Conclusions

Installation of the VIPA CDF VMEbus crates, TRACERs and VRB modules has taken place for a vertical slice test of CDF Run 2 electronics. All components are performing as defined.

VI. Acknowledgements

We would like to thank all the CDF physicists and engineers who participated in the numerous CDF Infrastructure meetings over the years which defined this readout system. Special thanks go to Greg Sullivan who co-authored the CDF/DOC/TRIGGER/CDFR/2388 document which provided the basis for this paper.

VII. References

[1] The CDF Collaboration, *Proposal for an Upgraded CDF Detector* , CDF/DOC/PUBLIC/1172, 1990.

[2] G. Drake, et al., CDF Front End Electronics: The Rabbit System, CDF/PUB/CDF/PUBLIC/0740, 1988.

[3] "The VMEbus Specification," Revised: 1987. Available from IEEE Transactions/Journals Dept., 445 Hoes Lane, Piscataway NY 08855.

[4] T. Shaw, Specification for CDF Custom 6U-to-9U Adapter Module, October 26, 1998.

[5] E. Barsotti, et al., Specification for: VME64 Extensions 10U & 7U Subracks for Physics, Document # ESE-SVX-960305.

[6] "VME64 Extensions(ANSI/VITA 1.1-1997)" Available from VITA7825 East Gelding Drive, Suite 104 Scottsdale, AZ 85260-3415, USA.

[7] MVME2301 is manufactured by Motorola, Inc. Motorola Computer Group, 2900 South Diablo Way, Tempe, AZ 85282.

[8] T. Shaw, Specification for TRigger And Clock + Event Readout Module (TRACER), April 24, 1998.

[9] CDF Group/Yale University, Trigger Supervisor Protocols for Run II, October 10, 1995.

[10] The Front-End/Trigger/DAQ upgrade group, The Clock for the CDF Upgrade CDF/DOC/PUBLIC/xxxx, 1993.

[11] T. Shaw, The Reset Crate, December 27, 1994.

[12] M. Bowden, et. al., VRB Readout Buffer/Fanout, Document # ESE-SVX-950719.